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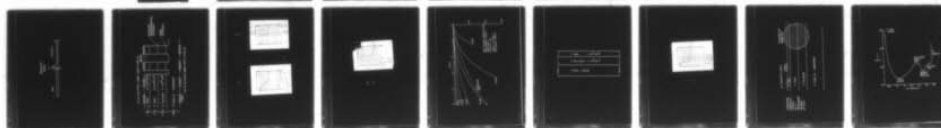
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RECTIFICATION AT NGAAS - N GA.7AL.3AS HETEROJUNCTIONS GROWN BY --ETC(U)  
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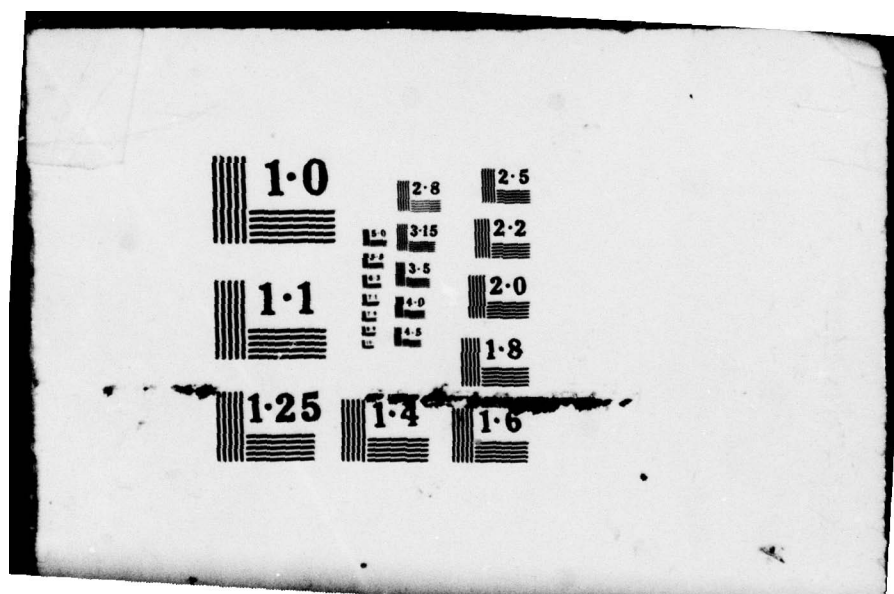
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**LEVEL II**RECTIFICATION AT nGaAs - nGa<sub>0.7</sub>Al<sub>0.3</sub>As HETEROJUNCTIONS

GROWN BY L.P.E.

by

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ABSTRACT

Heterojunctions between n-type GaAs ( $2 \times 10^{14} \text{ cm}^{-3}$ ),  $10^{17} \text{ cm}^{-3}$  and high purity n-type Ga<sub>0.7</sub>Al<sub>0.3</sub>As ( $1 \times 10^{15} \text{ cm}^{-3}$ ) have been grown by LPE at 700°C, and significant current rectification has been observed across them at room temperature. At low temperatures, the current drops and the degree of rectification increases considerably. The reverse current characteristic shows reasonable semi-quantitative agreement with theoretical I-V curves, calculated by using a thermionic emission model. The N-W profile measured across the interface indicates qualitatively the presence of a dipolar space-charge region, as expected.

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## INTRODUCTION

The nGaAs-n(Ga,Al)As heterojunction has been in recent years a subject of some controversy. The theory of Anderson<sup>1</sup> and of Oldham and Milnes<sup>2</sup> predicts that this heterojunction, which is largely free of interface states<sup>3</sup>, should possess an energy barrier in the conduction band edge, and thus exhibit current rectification. Experiments, however, have so far failed to show the expected rectifying behavior<sup>4,5</sup>, even though it is fairly certain from the quantum well experiments of Dingle et al.<sup>6</sup> and of Chang et al.<sup>7</sup> that the energy barriers exist. This has led to speculations on various fundamental mechanisms that might be controlling the current transport behavior across this heterojunction.<sup>4,8</sup>

We have recently grown nGaAs - nGa<sub>1-x</sub>Al<sub>x</sub>As heterojunctions by LPE and obtained significant rectification.<sup>9</sup>

Figure 1 shows a schematic of the conduction band edge profile across the n-n heterojunction.<sup>1,2</sup> For Ga<sub>1-x</sub>Al<sub>x</sub>As at  $x = .3$ , the energy step at an ideally abrupt interface is estimated to be about .33 eV at room temperature.<sup>6</sup> At equilibrium, electrons deplete from the Ga<sub>1-x</sub>Al<sub>x</sub>As to form a narrow accumulation region in the GaAs. A grading of the metallurgical interface lowers the barrier by an amount that increases with both the net doping in the Ga<sub>1-x</sub>Al<sub>x</sub>As and the interface transition

width.<sup>2</sup>

## EXPERIMENT AND RESULTS

Figure 2 shows a schematic of one of the two heterostructures we have examined. The three epilayers shown were grown by LPE on an  $n^+$  GaAs substrate, using a multiple well graphite horizontal sliding boat. The starting growth temperature was  $700^\circ\text{C}$ , and the growth rate was measured at about  $1000 \text{ \AA}/\text{minute}$ . The approximate layer thicknesses shown were measured by cleaving and staining. The carrier concentrations shown were not measured directly on these heterostructures, but correspond to the values which we obtain repeatably on thicker single layers of unintentionally doped GaAs and  $\text{Ga}_{.7}\text{Al}_{.3}\text{As}$ , grown under similar conditions.

The contact between the substrate and the  $(\text{Ga},\text{Al})\text{As}$  layer was expected and found to be ohmic. The  $10^{17} \text{ cm}^{-3}$  tin doped GaAs cap layer served as a contact layer on the other side of the heterojunction between the two high purity layers.

Gold-germanium dots, 10 mils in diameter, were evaporated and alloyed on both sides of the structure. They were tested to confirm their ohmic nature, following which mesas were etched to isolate the heterojunction interface areas below ohmic dots. Before etching, the contact resistance of the ohmic dots (type A) was meas-

ured to be about 12 ohms each. The I-V characteristics were then measured across the mesa heterostructure by applying a bias voltage to the mesa contact with respect to the grounded substrate.

Figure 3(a) and (b) show the typical room temperature rectification behavior observed, on different scales. The direction of rectification is consistent with theory. The forward current is limited mainly by the contact and lead resistances, demonstrating the substrate -  $\text{Ga}_{1-x}\text{Al}_x\text{As}$  interface to be a low resistance contact. The reverse current increases with the applied bias, showing a lack of saturation. This is because increasing the applied reverse voltage increases the interfacial electric field, which, for a finite transition width  $\ell$ , lowers the energy barrier.

We believe that the current across the heterojunction is largely due to thermionic emission over an energy barrier. We have not, as yet, made careful low temperature I-V measurements. However, we did make some quick observations by cooling the sample to liquid nitrogen and allowing it to warm slowly. Figure 4 shows the I-V characteristics at some unmeasured low temperature, probably between 100 and 200°K. It is observed that the current is lower by three orders of magnitude, and the rectification is significantly more pronounced, than at room temperature.

These characteristics were observed to be quite

insensitive to light.

#### COMPARISON WITH THEORY

To compare our results with theory, we modelled the heterojunction as two homogeneous bulk regions with a linearly graded transition region of width  $\ell$  sandwiched between them (Fig. 1). For mathematical simplicity, the integrated space charge in the transition region was assumed to be zero. We then solved Poisson's equation under conditions of applied bias to obtain the energy barriers to electron flow in either direction, and hence estimated the current voltage characteristics.<sup>10,11</sup> Fig. 5 shows the theoretically generated reverse I-V curves at room temperature, calculated for material parameters that correspond to the experimental values, using  $\ell$ , as a variable parameter. The dashed line is the experimental curve, and shows reasonable agreement with the  $\ell = 200 \text{ \AA}$  theoretical line, except at low bias.

We have not as yet measured the interface width. Garner et al.<sup>4</sup> have reported values of about  $100 \text{ \AA}$  for heterojunctions grown by LPE at  $750^\circ\text{C}$ .<sup>4</sup> A more definite knowledge of the interface width in our samples shall allow us to make a more meaningful comparison between experiment and theory and offer insights into the current transport mechanisms.

### FURTHER EXPERIMENTS AND RESULTS

A second heterostructure, shown in Fig. 6, with the  $\text{Ga}_{0.7}\text{Al}_{0.3}\text{As}$  layer interfaced with a  $10^{17}\text{cm}^{-3}$  tin doped GaAs layer was fabricated and tested in a manner similar to the structure shown in Fig. 2, except that the mesa cross section was 5 mil square. Again, rectification was observed in the I-V characteristics, which are shown in Fig. 7.

The reverse current in Fig. 7 shows a saturation 'knee'. If the barrier height was independent of the applied reverse voltage, then this would be the reverse saturation current. Calculations on our theoretical model show that this 'pseudo reverse saturation current' is roughly proportional to the net doping in the GaAs, while the rectification characteristics are otherwise largely insensitive to the GaAs doping. A comparison of Fig. 3(b) with Fig. 7 shows these theoretical predictions to be borne out by experiment.

Coming back to the first heterostructure (of Fig. 2), we decided to check the heterojunction interface for a dipolar space charge region, using conventional carrier density vs. depth profiling.<sup>12</sup> The sample, shown in Fig. 8, was prepared by using a self limiting anodic etch technique<sup>13</sup>, to ensure that the subsequently deposited Schottky barriers would punch through to the  $n^+$  substrate

before breakdown. A tin dot was then alloyed to the top surface to serve as the back contact. 10 mil diameter gold Schottky barriers were then deposited at a pressure below  $10^{-6}$  torr. Fig. 9 shows the N-W plot obtained, along with our interpretation of its various features. Note the presence of an accumulation region in the GaAs coupled with a depletion region in the  $\text{Ga}_{1-x}\text{Al}_x\text{As}$ . It should be cautioned that these results should not be regarded as anything better than qualitative. Also Kroemer and Harris<sup>14</sup> have observed a similar 'accumulation-depletion' dipolar region at n-n GaAs-(Ga,Al)As heterojunctions, but have failed to see rectification.

#### DISCUSSION

Of the various possible mechanisms for current transport across these rectifying heterojunctions, thermionic emission emerges as the leading candidate. Mechanisms that involve tunneling are improbable because the width of the depletion region energy barrier in the high purity  $\text{Ga}_{0.7}\text{Al}_{0.3}\text{As}$  is of the order of  $1000\text{\AA} - 3000\text{\AA}$ , too large for tunneling. Space charge recombination can be ruled out because the hole density is negligible. Space charge generation is possible; however, the extremely low density of interface states would suggest this mechanism to be unimportant.

The large temperature sensitivity of the I-V charac-

teristics backs thermionic emission over an energy barrier as being the main current transport mechanism. Such a barrier, of course, is expected to result from the heterojunction bandedge mismatch theory. However, other possibilities should be examined. For instance, Oldham and Milnes<sup>15</sup> have shown how a large interface state density can pin the Fermi level at the interface, creating a depletion region on both sides of the interface. The I-V characteristics, in such a case, would show reverse behavior in both directions, and the N-W characteristics would presumably show no accumulation region. Besides, Lang and Logan<sup>3</sup> have measured the interface state density on their LPE grown samples to be less than  $10^9 \text{ cm}^{-2}$ , which is far too low to affect the band bending.

A second possibility, that of a p conversion region at or near the interface is also very unlikely, mainly because such a structure would not account for the observed I-V behavior.

#### ACKNOWLEDGEMENTS

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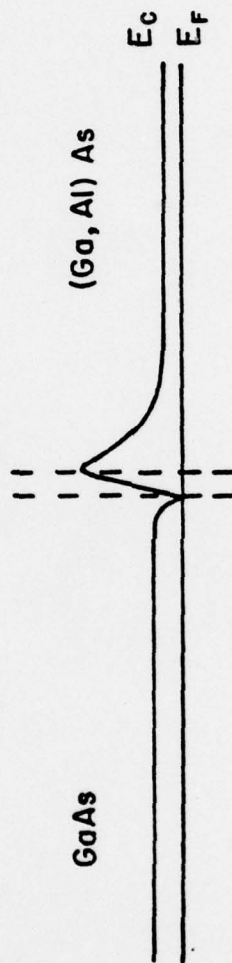
FIGURE CAPTIONS

- Fig. 1 - Schematic of the conduction band edge profile across the  $\text{nGaAs:n(Ga,Al)As}$  graded gap heterojunction.
- Fig. 2 - Schematic diagram of heterostructure examined for rectification.
- Fig. 3 - (a) & (b) - Room temperature I-V characteristics measured across the structure in Fig. 2. The substrate was grounded, and the voltage  $V$  applied to a mesa contact.
- Fig. 4 - Low temperature (unmeasured, 100-200°K) I-V characteristics of structure in Fig. 2.
- Fig. 5 - Theoretically calculated reverse I-V characteristics of a heterojunction with material parameters corresponding to the experimental values. The experimental curve is also plotted for comparison.
- Fig. 6 - A second heterostructure in which the  $\text{Ga}_{.7}\text{Al}_{.3}\text{As}$  interfaces a  $10^{17}\text{cm}^{-3}$  doped GaAs layer, that was examined. The size of the ohmic dots alloyed to this structure was 5 mil square ( $\sim 1/\pi$  of the area of dots in first structure).
- Fig. 7 - Room temperature I-V characteristics of the structure in Fig. 6. Note the reverse saturation knee at about - .5 mA.

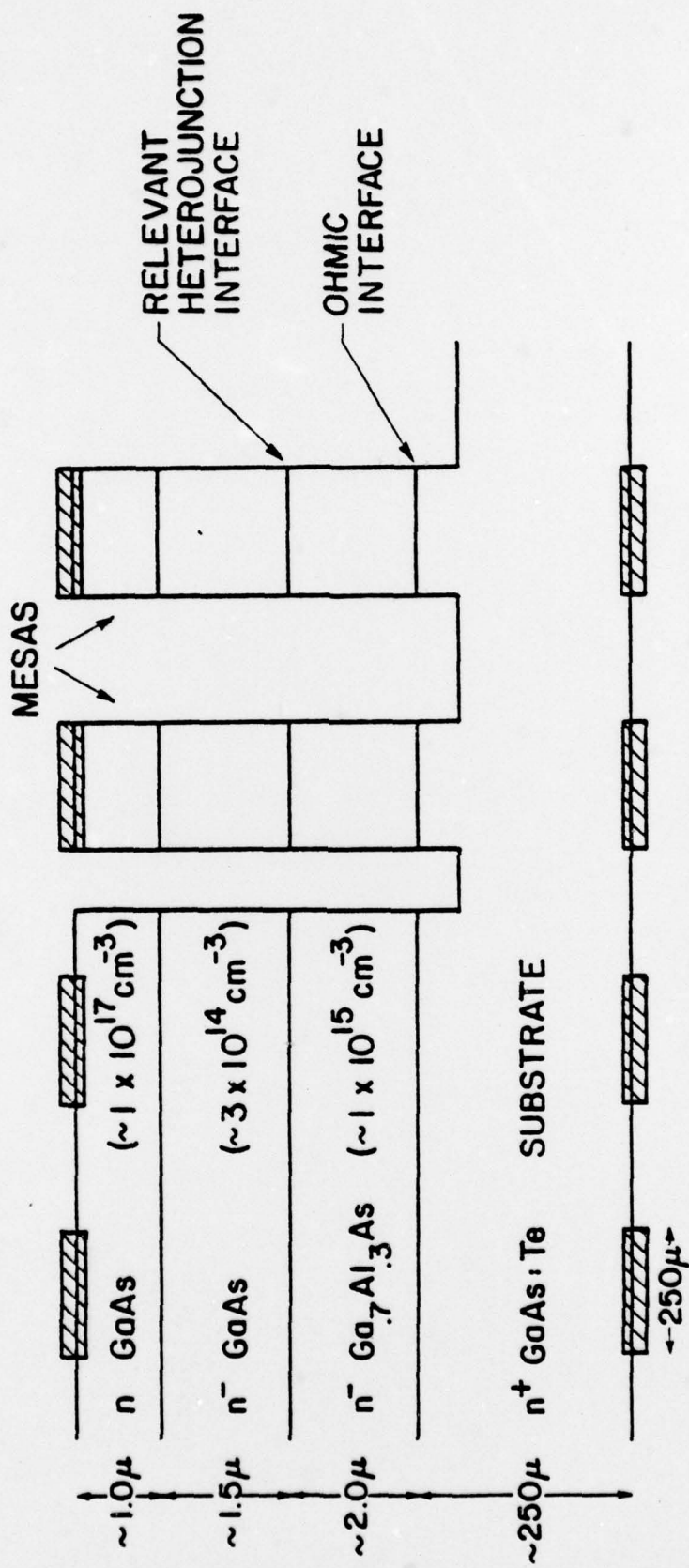
Fig. 8 - Schottky diodes fabricated for measuring the carrier density vs. depth (N-W) profile across the heterojunction.

Fig. 9 - N-W profile measured across the heterostructure using a junction profiler. This measurement should, at best, be regarded as qualitative.

TRANSITION  
REGION



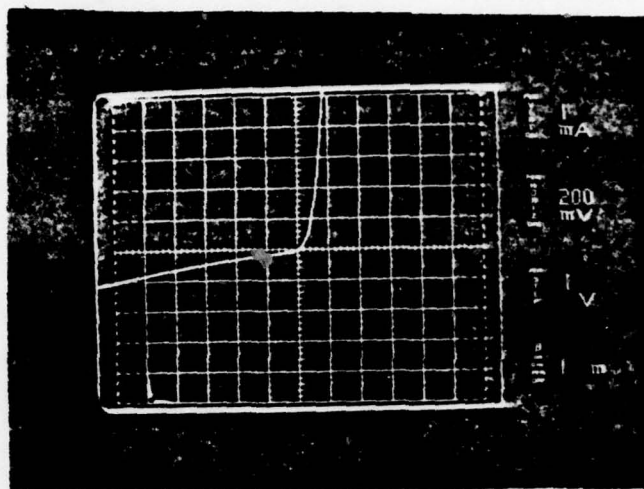
Au-Ge ALLOYED OHMIC DOTS (TYPE A)



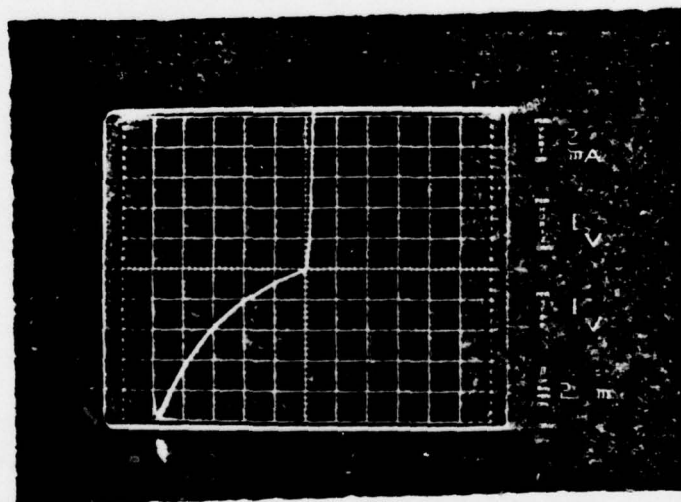
Au-Ge ALLOYED OHMIC DOTS (TYPE B)



3(a)



3(b)



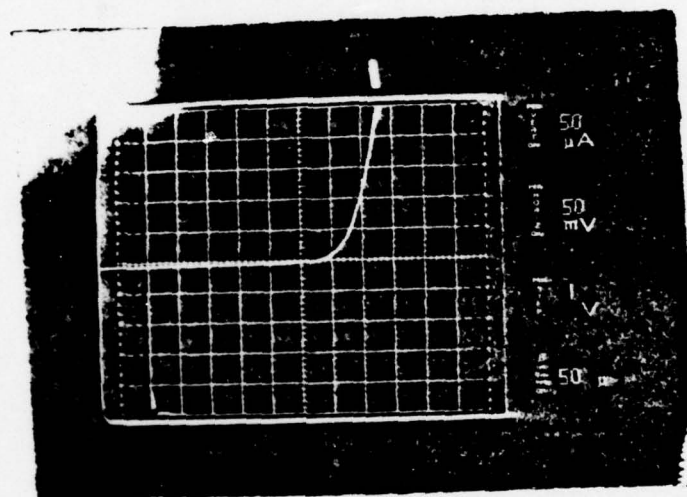
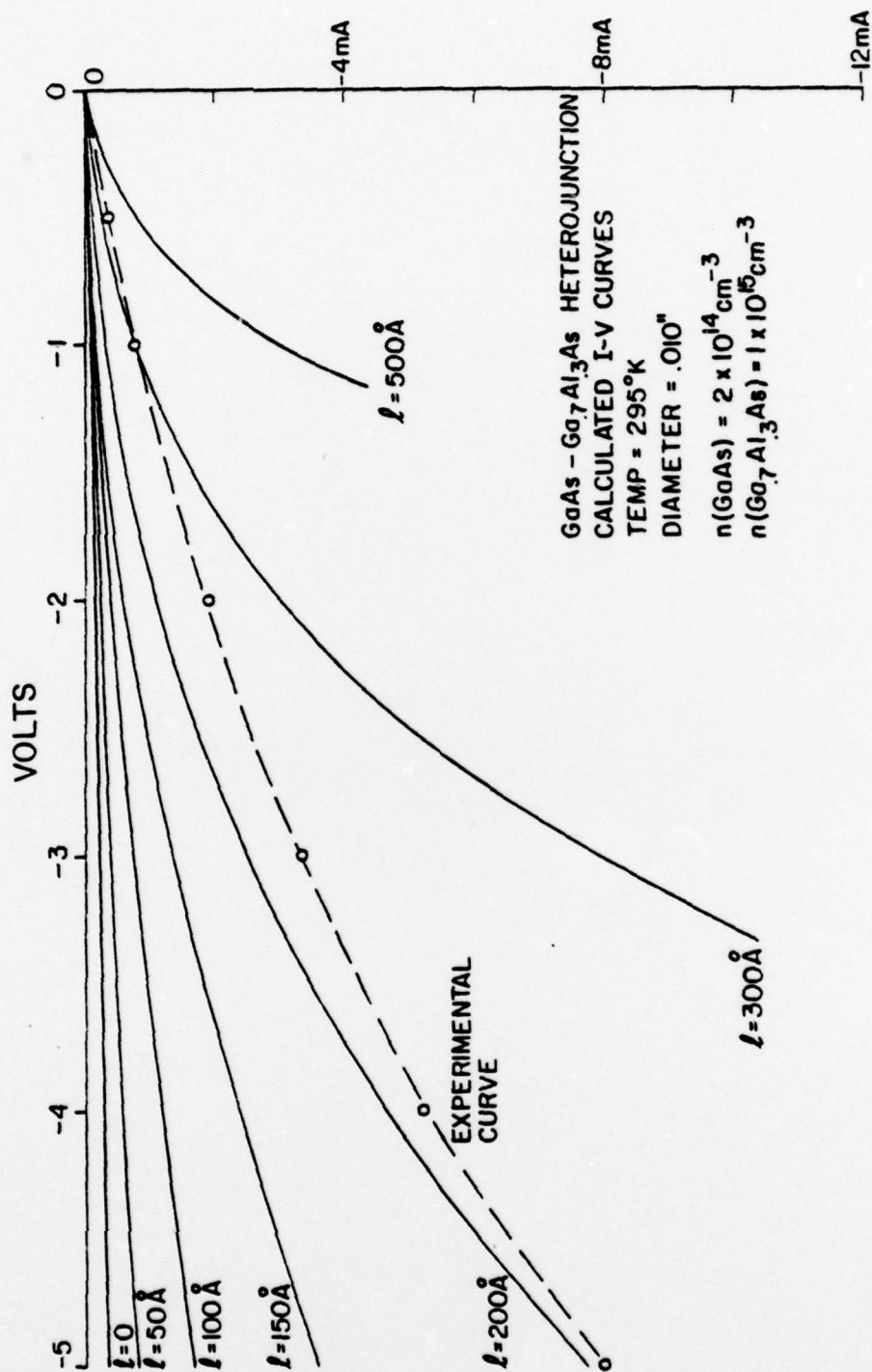


Fig 4



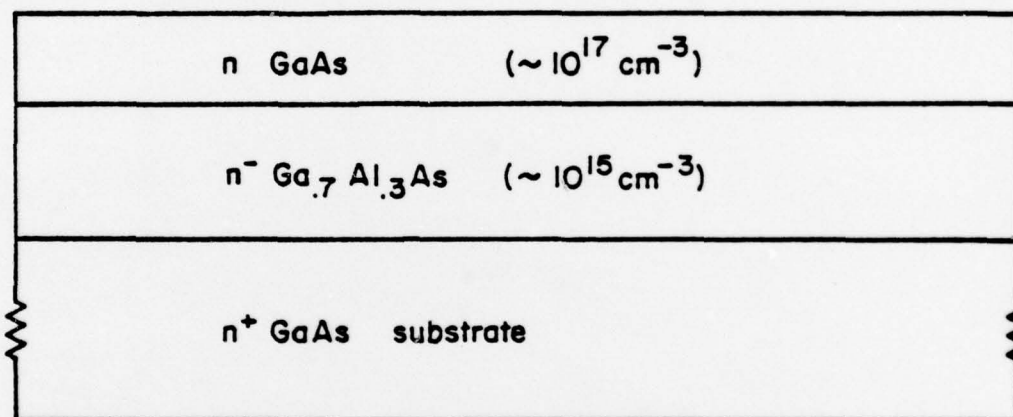
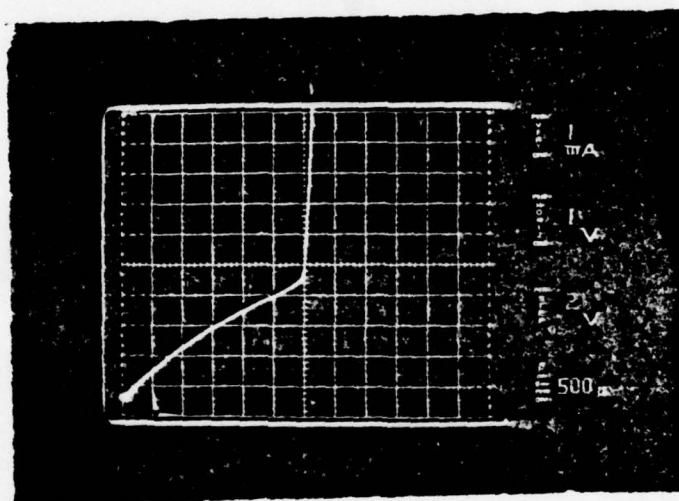


Fig 6



ALLOYED TIN  
OHMIC DOT

Au SCHOTTKY DOTS

←250μ→

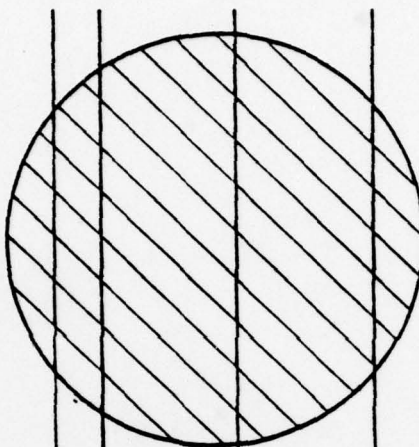
n GaAs

n<sup>-</sup> GaAs

n<sup>-</sup> Ga<sub>0.7</sub>Al<sub>0.3</sub>As

n<sup>+</sup> GaAs: Te SUBSTRATE

STRUCTURE  
ANODICALLY  
ETCHED  
TO A  
BREAKDOWN  
VOLTAGE  
OF 90 V.



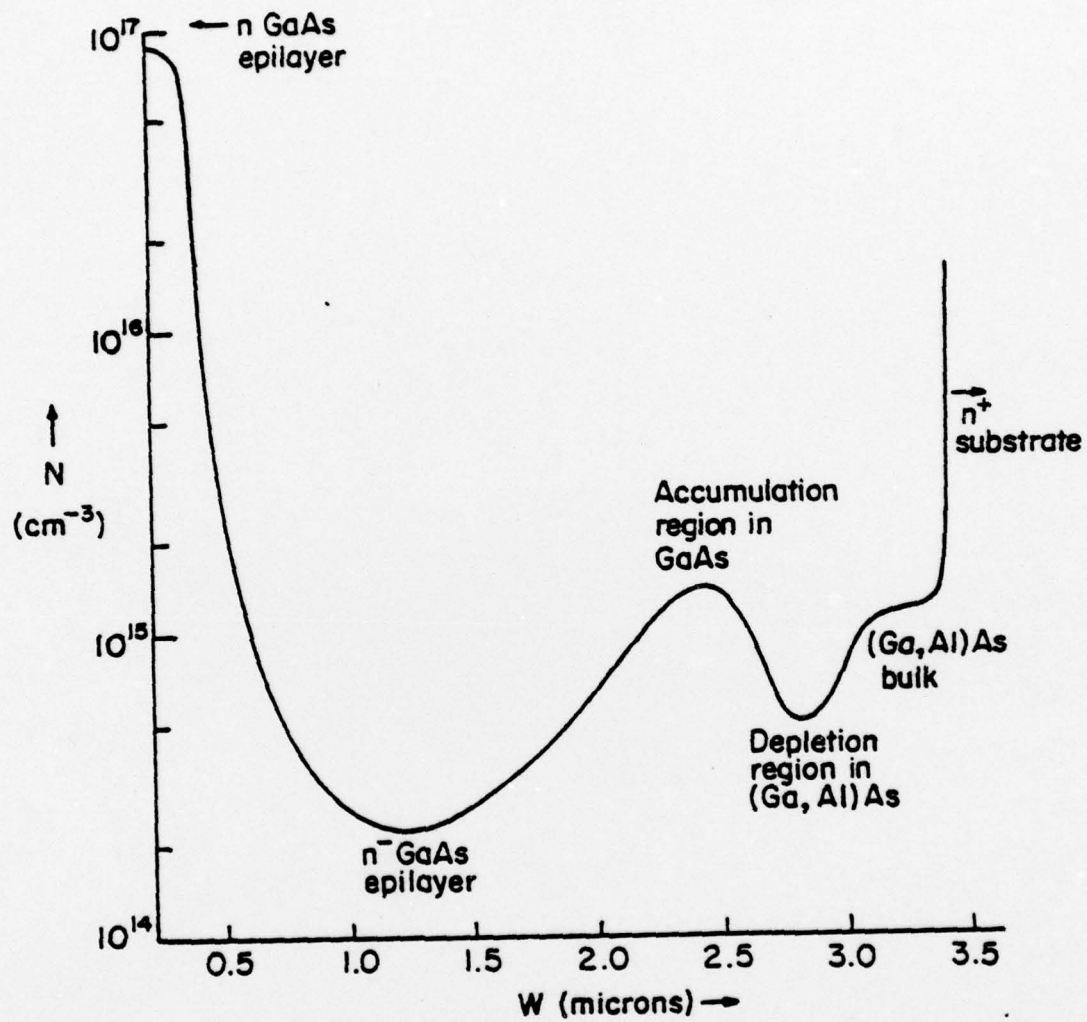


Fig 1